Cornell University

ECE4750/CS4420 Computer Architecture L9-1: Tomasulo Examples

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Tomasulo: Example

Instruction	Instr. Status I	E	W
`fld1 f6,34($2)`			
`fld2 f2,45($3)`			
`fmul f0,f2,f4`			
`fsub f8,f6,f2`			
`fdiv f10,f0,f6`			
`fadd f6,f8,f2`			

Reservation Stations

	Busy	Op	Vj	Vk	Qj	Qk	A
Load1							
Load2							
Add1							
Add2							
Add3							
Mul1							
Mul2							

Register Result Status

	F0	F2	F4	F6	F8	F10	F12	...	F30
Qi									

Clock:

Tomasulo: Example

Instruction	Instr. Status I	E	W
`fld1 f6,34($2)`	1		
`fld2 f2,45($3)`			
`fmul f0,f2,f4`			
`fsub f8,f6,f2`			
`fdiv f10,f0,f6`			
`fadd f6,f8,f2`			

Reservation Stations

	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	Y	ld	$2				34
Load2							
Add1							
Add2							
Add3							
Mul1							
Mul2							

Register Result Status

	F0	F2	F4	F6	F8	F10	F12	...	F30
Qi				Load1					

Clock: 1

Tomasulo: Example

Instruction	Instr. Status I	E	W
`fld1 f6,34($2)`	1		
`fld2 f2,45($3)`	2		
`fmul f0,f2,f4`			
`fsub f8,f6,f2`			
`fdiv f10,f0,f6`			
`fadd f6,f8,f2`			

Reservation Stations

		Busy	Op	Vj	Vk	Qj	Qk	A
Load1	1	Y	ld	$2				$2+34
Load2		Y	ld	$3				45
Add1								
Add2								
Add3								
Mul1								
Mul2								

Register Result Status

	F0	F2	F4	F6	F8	F10	F12	...	F30
Qi		Load2		Load1					

Clock: 2

Tomasulo: Example

	Instruction	Instr. Status I	E	W
0	`fld1 f6,34($2)`	1	3	
1	`fld2 f2,45($3)`	2		
	`fmul f0,f2,f4`	3		
	`fsub f8,f6,f2`			
	`fdiv f10,f0,f6`			
	`fadd f6,f8,f2`			

Reservation Stations

	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	Y	ld	$2				$2+34
Load2	Y	ld	$3				$3+45
Add1							
Add2							
Add3							
Mul1	Y	fmul		f4	Load2		
Mul2							

Register Result Status (also values)

	F0	F2	F4	F6	F8	F10	F12	...	F30
Qi	Mul1	Load2		Load1					

Clock: 3

Tomasulo: Example

	Instruction	Instr. Status I	E	W	
	`fld1 f6,34($2)`	1	3	4	
0	`fld2 f2,45($3)`	2	4		
	`fmul f0,f2,f4`	3			
	`fsub f8,f6,f2`	4			
	`fdiv f10,f0,f6`				
	`fadd f6,f8,f2`				

Reservation Stations

	Busy	Op	Vj	Vk	Qj	Qk	A
Load1	-	-	-				-
Load2	Y	ld	$3				$3+45
Add1	Y	fsub	M1			Load2	
Add2							
Add3							
Mul1	Y	fmul		f4	Load2		
Mul2							

Register Result Status (also values)

	F0	F2	F4	F6	F8	F10	F12	...	F30
Qi	Mul1	Load2		M1	Add1				

Clock: 4

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4		
fdiv f10,f0,f6	5		
fadd f6,f8,f2			

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$	-	-	-				-
2 Add$_1$	Y	fsub	M_1	M_2		-	
Add$_2$							
Add$_3$							
10 Mul$_1$	Y	fmul	M_2	f4	-		
Mul$_2$	Y	fdiv		M_1	Mul_1		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul_1	M_2		M_1	Add_1	Mul_2			

Clock: 5

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4		
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6		

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
1 Add$_1$	Y	fsub	M_1	M_2			
Add$_2$	Y	fadd		M_2	Add_1		
Add$_3$							
9 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul_1		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul_1	M_2		Add_2	Add_1	Mul_2			

Clock: 6

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6		

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
0 Add$_1$	Y	fsub	M_1	M_2			
Add$_2$	Y	fadd		M_2	Add_1		
Add$_3$							
8 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul_1		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul_1	M_2		Add_2	Add_1	Mul_2			

Clock: 7

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6		

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$	-	-	-	-			
2 Add$_2$	Y	fadd	M_1- M_2	M_2			-
Add$_3$							
7 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul_1		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul_1	M_2		Add_2	M_1- M_2	Mul_2			

Clock: 8

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6		

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
1 Add$_2$	Y	fadd	M_1- M_2	M_2			
Add$_3$							
6 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul_1		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul_1	M_2		Add_2	M_1- M_2	Mul_2			

Clock: 9

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6	10	

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
0 Add$_2$	Y	fadd	M_1- M_2	M_2			
Add$_3$							
5 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul_1		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul_1	M_2		Add_2	M_1- M_2	Mul_2			

Clock: 10

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6	10	11

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$	-	-	-	-			
Add$_3$							
4 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul$_1$		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul$_1$	M_2		M_1	M_1- M_2	Mul$_2$			

Clock: 11

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6	10	11

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
3 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul$_1$		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul$_1$	M_2		M_1	M_1- M_2	Mul$_2$			

Clock: 12

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6	10	11

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
2 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul$_1$		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul$_1$	M_2		M_1	M_1- M_2	Mul$_2$			

Clock: 13

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3		
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6	10	11

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
1 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul$_1$		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul$_1$	M_2		M_1	M_1- M_2	Mul$_2$			

Clock: 14

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3	15	
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6	10	11

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
0 Mul$_1$	Y	fmul	M_2	f4			
Mul$_2$	Y	fdiv		M_1	Mul$_1$		

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	Mul$_1$	M_2		M_1	M_1- M_2	Mul$_2$			

Clock: 15

Tomasulo: Example

Instruction	I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3	15	16
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5		
fadd f6,f8,f2	6	10	11

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$	-	-	-	-			
40 Mul$_2$	Y	fdiv	M_2xf4	M_1			

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	M_2xf4	M_2		M_1	M_1- M_2	Mul$_2$			

Clock: 16

Tomasulo: Example

Instruction	Instr. Status I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3	15	16
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5	56	
fadd f6,f8,f2	6	10	11

Reservation Stations

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$							
Mul$_2$	Y	fdiv	M_2xf4		M_1		

Register Result Status (also values)

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	M_2xf4	M_2		M_1	M_1- M_2	Mul$_2$			

Clock: 56

Tomasulo: Example

Instruction	Instr. Status I	E	W
fld$_1$ f6,34($2)	1	3	4
fld$_2$ f2,45($3)	2	4	5
fmul f0,f2,f4	3	15	16
fsub f8,f6,f2	4	7	8
fdiv f10,f0,f6	5	56	57
fadd f6,f8,f2	6	10	11

Reservation Stations

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$							
Mul$_2$	-	-	-	-			

Register Result Status (also values)

	F0	F2	F4	F6	F8	F10	F12	...	F30
Q_i	M_2xf4	M_2		M_1	M_1- M_2	M_2xf4/M_1			

Clock: 57

Tomasulo: Loop Example

- Renaming powerful tool across loops
  - Scoreboard unable to process multiple iterations simultaneously
- Hardware loop unrolling
  - process several loop iterations simultaneously
  - make it transparent to the compiler

```
L: fld f0,0($1)
   fmul f4,f0,f2
   fsd f4,0($1)
   subi $1,$1,8
   bne $1,$0,L
```


Tomasulo: Loop Example

Instruction	Instr. Status I	E	W
fld$_1$ f0,0($1)			
fmul$_1$ f4,f0,f2			
fsd$_1$ f4,0($1)			
fld$_2$ f0,0($1)			
fmul$_2$ f4,f0,f2			
fsd$_2$ f4,0($1)			

Reservation Stations

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$							
Mul$_2$							
Store$_1$							
Store$_2$							

Register Result Status

	F0	F2	F4
Q_i			

$1: Clock:

Tomasulo: Loop Example

Instruction	Instr. Status I	E	W
fld$_1$ f0,0($1)	1		
fmul$_1$ f4,f0,f2			
fsd$_1$ f4,0($1)			
fld$_2$ f0,0($1)			
fmul$_2$ f4,f0,f2			
fsd$_2$ f4,0($1)			

Reservation Stations

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$	Y	fld	16				0
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$							
Mul$_2$							
Store$_1$							
Store$_2$							

Register Result Status

	F0	F2	F4
Q_i	Load$_1$		

$1: 16 Clock: 1

Tomasulo: Loop Example

Instruction	Instr. Status I	E	W
fld$_1$ f0,0($1)	1		
fmul$_1$ f4,f0,f2	2		
fsd$_1$ f4,0($1)			
fld$_2$ f0,0($1)			
fmul$_2$ f4,f0,f2			
fsd$_2$ f4,0($1)			

Reservation Stations

	Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$	Y	fld	16				16
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$	Y	fmul		f2	Load$_1$		
Mul$_2$							
Store$_1$							
Store$_2$							

Register Result Status

	F0	F2	F4
Q_i	Load$_1$		Mul$_1$

$1: 16 Clock: 2

Tomasulo: Loop Example

	Instruction	I	E	W
	fld$_1$ f0,0($1)	1		
	fmul$_1$ f4,f0,f2	2		
	fsd$_1$ f4,0($1)	3		
	fld$_2$ f0,0($1)			
	fmul$_2$ f4,f0,f2			
	fsd$_2$ f4,0($1)			

		Busy	Op	V_j	V_k	Q_j	Q_k	A
6	Load$_1$	Y	fld	16				16
	Load$_2$							
	Add$_1$							
	Add$_2$							
	Add$_3$							
	Mul$_1$	Y	fmul		f2	Load$_1$		
	Mul$_2$							
	Store$_1$	Y	fsd	16			Mul$_1$	0
	Store$_2$							

Register Result Status	F0	F2	F4
Q_i	Load$_1$		Mul$_1$

$1	Clock
16	3

Tomasulo: Loop Example

	Instruction	I	E	W
	fld$_1$ f0,0($1)	1		
	fmul$_1$ f4,f0,f2	2		
	fsd$_1$ f4,0($1)	3		
	fld$_2$ f0,0($1)			
	fmul$_2$ f4,f0,f2			
	fsd$_2$ f4,0($1)			

		Busy	Op	V_j	V_k	Q_j	Q_k	A
5	Load$_1$	Y	fld	16				16
	Load$_2$							
	Add$_1$							
	Add$_2$							
	Add$_3$							
	Mul$_1$	Y	fmul		f2	Load$_1$		
	Mul$_2$							
	Store$_1$	Y	fsd	16			Mul$_1$	16
	Store$_2$							

Register Result Status	F0	F2	F4
Q_i	Load$_1$		Mul$_1$

```
subi $1,$1,8
```

$1	Clock
8	4

Tomasulo: Loop Example

	Instruction	I	E	W
	fld$_1$ f0,0($1)	1		
	fmul$_1$ f4,f0,f2	2		
	fsd$_1$ f4,0($1)	3		
	fld$_2$ f0,0($1)			
	fmul$_2$ f4,f0,f2			
	fsd$_2$ f4,0($1)			

		Busy	Op	V_j	V_k	Q_j	Q_k	A
4	Load$_1$	Y	fld	16				16
	Load$_2$							
	Add$_1$							
	Add$_2$							
	Add$_3$							
	Mul$_1$	Y	fmul		f2	Load$_1$		
	Mul$_2$							
	Store$_1$	Y	fsd	16			Mul$_1$	16
	Store$_2$							

Register Result Status	F0	F2	F4
Q_i	Load$_1$		Mul$_1$

```
bne $1,$0,L
```

$1	Clock
8	5

Tomasulo: Loop Example

	Instruction	I	E	W
	fld$_1$ f0,0($1)	1		
	fmul$_1$ f4,f0,f2	2		
	fsd$_1$ f4,0($1)	3		
	fld$_2$ f0,0($1)	6		
	fmul$_2$ f4,f0,f2			
	fsd$_2$ f4,0($1)			

		Busy	Op	V_j	V_k	Q_j	Q_k	A
3	Load$_1$	Y	fld	16				16
	Load$_2$	Y	fld	8				0
	Add$_1$							
	Add$_2$							
	Add$_3$							
	Mul$_1$	Y	fmul		f2	Load$_1$		
	Mul$_2$							
	Store$_1$	Y	fsd	16			Mul$_1$	16
	Store$_2$							

Register Result Status	F0	F2	F4
Q_i	Load$_2$		Mul$_1$

$1	Clock
8	6

Tomasulo: Loop Example

	Instruction	I	E	W
	fld$_1$ f0,0($1)	1		
	fmul$_1$ f4,f0,f2	2		
	fsd$_1$ f4,0($1)	3		
	fld$_2$ f0,0($1)	6		
	fmul$_2$ f4,f0,f2	7		
	fsd$_2$ f4,0($1)			

		Busy	Op	V_j	V_k	Q_j	Q_k	A
2	Load$_1$	Y	fld	16				16
	Load$_2$	Y	fld	8				8
	Add$_1$							
	Add$_2$							
	Add$_3$							
	Mul$_1$	Y	fmul		f2	Load$_1$		
	Mul$_2$	Y	fmul		f2	Load$_2$		
	Store$_1$	Y	fsd	16			Mul$_1$	16
	Store$_2$							

Register Result Status	F0	F2	F4
Q_i	Load$_2$		Mul$_2$

$1	Clock
8	7

Tomasulo: Loop Example

	Instruction	I	E	W
	fld$_1$ f0,0($1)	1		
	fmul$_1$ f4,f0,f2	2		
	fsd$_1$ f4,0($1)	3		
	fld$_2$ f0,0($1)	6		
	fmul$_2$ f4,f0,f2	7		
	fsd$_2$ f4,0($1)	8		

		Busy	Op	V_j	V_k	Q_j	Q_k	A
1	Load$_1$	Y	fld	16				16
	Load$_2$	Y	fld	8				8
	Add$_1$							
	Add$_2$							
	Add$_3$							
	Mul$_1$	Y	fmul		f2	Load$_1$		
	Mul$_2$	Y	fmul		f2	Load$_2$		
	Store$_1$	Y	fsd	16			Mul$_1$	16
	Store$_2$	Y	fsd	8			Mul$_2$	0

Register Result Status	F0	F2	F4
Q_i	Load$_2$		Mul$_2$

$1	Clock
8	8

Tomasulo: Loop Example

	Instruction	I	E	W
	`fld1 f0,0($1)`	1	9	
	`fmul1 f4,f0,f2`	2		
	`fsd1 f4,0($1)`	3		
	`fld2 f0,0($1)`	6		
	`fmul2 f4,f0,f2`	7		
	`fsd2 f4,0($1)`	8		

		Busy	Op	V_j	V_k	Q_j	Q_k	A
0	$Load_1$	Y	fld	16				16
1	$Load_2$	Y	fld	8				8
	Add_1							
	Add_2							
	Add_3							
	Mul_1	Y	fmul		f2	$Load_1$		
	Mul_2	Y	fmul		f2	$Load_2$		
	$Store_1$	Y	fsd	16			Mul_1	16
	$Store_2$	Y	fsd	8			Mul_2	8

Register Result Status	F0	F2	F4
Q_i	$Load_2$		Mul_2

`subi $1,$1,8`

$1	Clock
0	9

Tomasulo: Loop Example

	Instruction	I	E	W
	`fld1 f0,0($1)`	1	9	10
	`fmul1 f4,f0,f2`	2		
	`fsd1 f4,0($1)`	3		
	`fld2 f0,0($1)`	6	10	
	`fmul2 f4,f0,f2`	7		
	`fsd2 f4,0($1)`	8		

		Busy	Op	V_j	V_k	Q_j	Q_k	A
	$Load_1$	-	-	-				-
0	$Load_2$	Y	fld	8				8
	Add_1							
	Add_2							
	Add_3							
10	Mul_1	Y	fmul	M_1	f2	-		
	Mul_2	Y	fmul		f2	$Load_2$		
	$Store_1$	Y	fsd	16			Mul_1	16
	$Store_2$	Y	fsd	8			Mul_2	8

Register Result Status	F0	F2	F4
Q_i	$Load_2$		Mul_2

`bne $1,$0,L`

$1	Clock
0	10

Tomasulo: Loop Example

	Instruction	I	E	W
	`fld1 f0,0($1)`	1	9	10
	`fmul1 f4,f0,f2`	2		
	`fsd1 f4,0($1)`	3		
	`fld2 f0,0($1)`	6	10	11
	`fmul2 f4,f0,f2`	7		
	`fsd2 f4,0($1)`	8		

		Busy	Op	V_j	V_k	Q_j	Q_k	A
	$Load_1$							
	$Load_2$	-	-	-				-
	Add_1							
	Add_2							
	Add_3							
9	Mul_1	Y	fmul	M_1	f2			
10	Mul_2	Y	fmul	M_2	f2	-		
	$Store_1$	Y	fsd	16			Mul_1	16
	$Store_2$	Y	fsd	8			Mul_2	8

Register Result Status	F0	F2	F4
Q_i	$Load_2$		Mul_2

$1	Clock
0	11

Tomasulo: Loop Example

	Instruction	I	E	W
	`fld1 f0,0($1)`	1	9	10
	`fmul1 f4,f0,f2`	2	20	
	`fsd1 f4,0($1)`	3		
	`fld2 f0,0($1)`	6	10	11
	`fmul2 f4,f0,f2`	7		
	`fsd2 f4,0($1)`	8		

		Busy	Op	V_j	V_k	Q_j	Q_k	A
	$Load_1$							
	$Load_2$							
	Add_1							
	Add_2							
	Add_3							
0	Mul_1	Y	fmul	M_1	f2			
1	Mul_2	Y	fmul	M_2	f2			
	$Store_1$	Y	fsd	16			Mul_1	16
	$Store_2$	Y	fsd	8			Mul_2	8

Register Result Status	F0	F2	F4
Q_i	$Load_2$		Mul_2

$1	Clock
0	20

Tomasulo: Loop Example

	Instruction	I	E	W
	`fld1 f0,0($1)`	1	9	10
	`fmul1 f4,f0,f2`	2	20	21
	`fsd1 f4,0($1)`	3		
	`fld2 f0,0($1)`	6	10	11
	`fmul2 f4,f0,f2`	7	21	
	`fsd2 f4,0($1)`	8		

		Busy	Op	V_j	V_k	Q_j	Q_k	A
	$Load_1$							
	$Load_2$							
	Add_1							
	Add_2							
	Add_3							
	Mul_1	-	-	-	-			
0	Mul_2	Y	fmul	M_2	f2			
1	$Store_1$	Y	fsd	16	M_1xf2		-	16
	$Store_2$	Y	fsd	8			Mul_2	8

Register Result Status	F0	F2	F4
Q_i	$Load_2$		Mul_2

$1	Clock
0	21

Tomasulo: Loop Example

	Instruction	I	E	W
	`fld1 f0,0($1)`	1	9	10
	`fmul1 f4,f0,f2`	2	20	21
	`fsd1 f4,0($1)`	3	22	
	`fld2 f0,0($1)`	6	10	11
	`fmul2 f4,f0,f2`	7	21	22
	`fsd2 f4,0($1)`	8		

		Busy	Op	V_j	V_k	Q_j	Q_k	A
	$Load_1$							
	$Load_2$							
	Add_1							
	Add_2							
	Add_3							
	Mul_1							
	Mul_2	-	-	-	-			
0	$Store_1$	Y	fsd	16	M_1xf2			16
1	$Store_2$	Y	fsd	8	M_2xf2		-	8

Register Result Status	F0	F2	F4
Q_i	$Load_2$		Mul_2

$1	Clock
0	22

Tomasulo: Loop Example

Instruction	Instr. Status I	E	W
fld$_1$ f0,0($1)	1	9	10
fmul$_1$ f4,f0,f2	2	20	21
fsd$_1$ f4,0($1)	3	22	23
fld$_2$ f0,0($1)	6	10	11
fmul$_2$ f4,f0,f2	7	21	22
fsd$_2$ f4,0($1)	8	23	

	Reservation Stations Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$							
Mul$_2$							
Store$_1$	-	-	-	-			-
0 Store$_2$	Y	fsd	8	M_2xf2		-	8

Register Result Status	F0	F2	F4
Q_i	Load$_2$		Mul$_2$

$1	Clock
0	23

Tomasulo: Loop Example

Instruction	Instr. Status I	E	W
fld$_1$ f0,0($1)	1	9	10
fmul$_1$ f4,f0,f2	2	20	21
fsd$_1$ f4,0($1)	3	22	23
fld$_2$ f0,0($1)	6	10	11
fmul$_2$ f4,f0,f2	7	21	22
fsd$_2$ f4,0($1)	8	23	24

	Reservation Stations Busy	Op	V_j	V_k	Q_j	Q_k	A
Load$_1$							
Load$_2$							
Add$_1$							
Add$_2$							
Add$_3$							
Mul$_1$							
Mul$_2$							
Store$_1$							
Store$_2$	-	-	-	-			-

Register Result Status	F0	F2	F4
Q_i	Load$_2$		Mul$_2$

$1	Clock
0	24