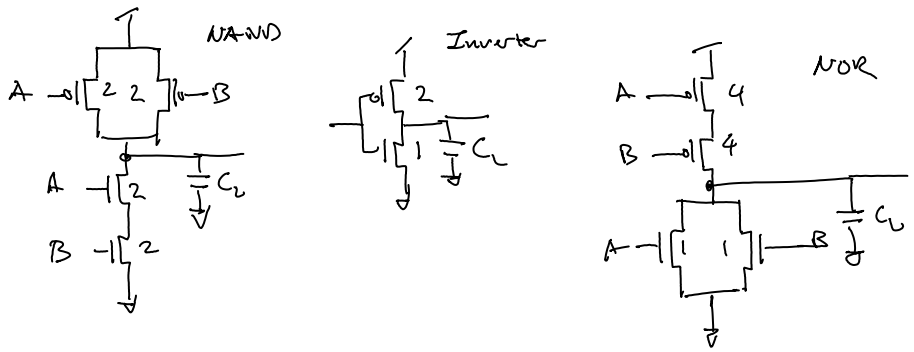
Logical Effort

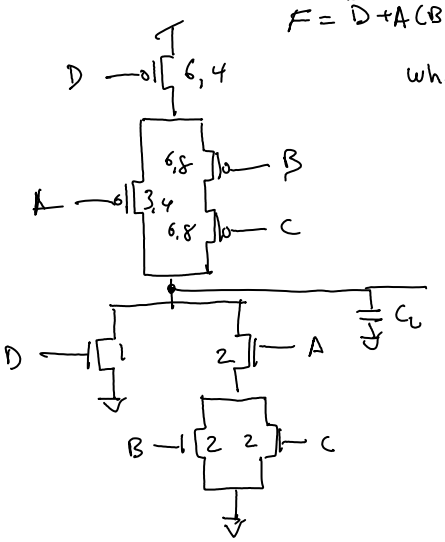
Friday, March 05, 2010
08:57

CMOS Logic

worst-case t_{pLH}, t_{pHL}

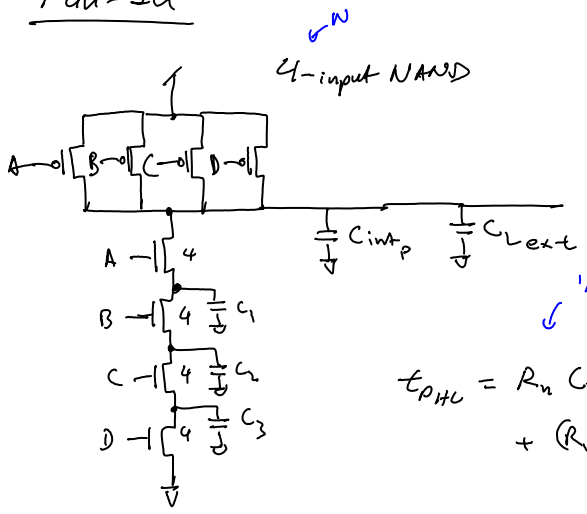


$F = \overline{D + A(B+C)}$



Which sizing is better, and why?

Fan-In



1/4 of the R_N of an inverter

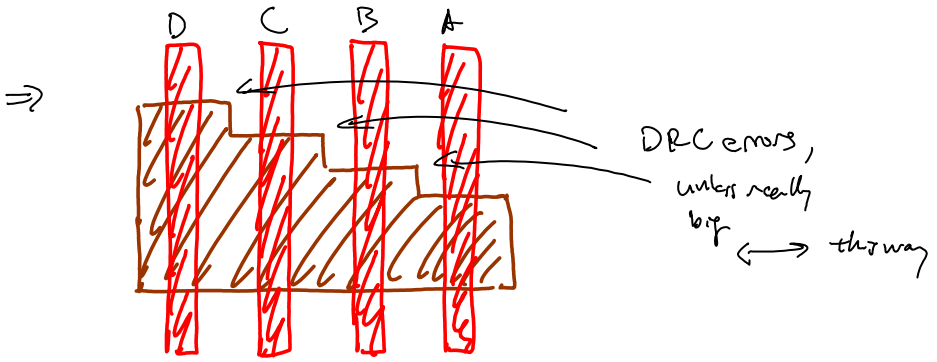
$$t_{pHL} = R_n C_3 + (R_n + R_n) C_2 + (R_n + R_n + R_n) C_1 + (R_n + R_n + R_n + R_n)(C_L + C_{int,p})$$

αN ; $N \cdot C_{db,pmos}$

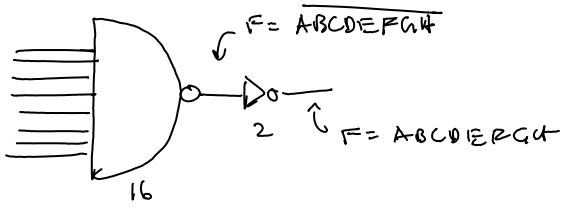
$\Rightarrow t_{pHL} \propto N$

you could size things differently, like make D the biggest and A the smallest

$M_D > M_C > M_B > M_A$

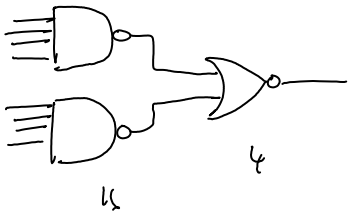


We could also make use of knowledge about the last incoming signal:



Breaking Up Gates

OR



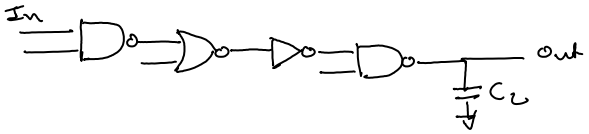
Or, you could reduce the output swing and let the restoring effect of the inverter fix it.

Logical Effort

for an inverter

$$t_p = t_{p_0}\left(1 + \frac{f}{\gamma}\right)$$

$$= 0.69\, R_{inv}\,(C_{int} + C_{ext})$$



fanout of NAND

$$t_{NAND} = 0.69\, R_{NAND}\,(C_{int,NAND} + C_{ext})$$

$$= 0.69\, R_{NAND}\, C_{int,NAND} + 0.69\, R_{NAND} \cdot C_{gate,NAND}\left(\frac{C_{ext}}{C_{gate,NAND}}\right)$$

t_{NAND} = $0.69\, R_{NAND}\, C_{int,NAND}$ $0.69\, R_{NAND}\, C_{gate,NAND}$. C_{ext}

$$\frac{t_{NAND}}{t_{inv}} = \frac{0.69 R_{NAND} C_{int,NAND}}{0.69 R_{inv} C_{g,inv}} + \frac{0.69 R_{NAND} C_{gate,NAND}}{0.69 R_{inv} C_{g,inv}} \cdot \frac{C_{ext}}{C_{g,NAND}}$$

$C_{ext,NAND}$

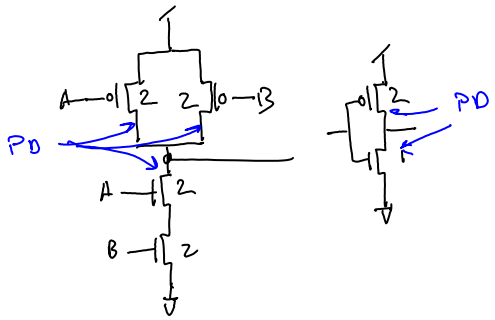
$$D_{NAND} = \frac{t_{NAND}}{t_{inv}} = \frac{C_{int,NAND}}{C_{gate,inv}} + \frac{C_{gate,NAND}}{C_{gate,inv}} FO_{NAND}$$

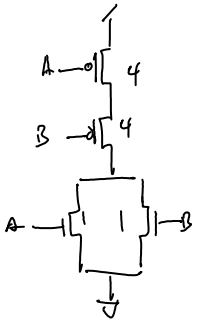
parasitic delay — Logical effort

$$D_{NAND} = PD_{NAND} + LE_{NAND} FO_{NAND}$$

$$LE_{2NAND} = \frac{2+2}{2+1} = \frac{4}{3}$$

$$PD_{2NAND} = \frac{2+2+2}{2+1} = 2$$





$$LE_{2NOR} = \frac{4+1}{2+1} = \frac{5}{3}$$

$$PD_{2NOR} = \frac{4+1+1}{2+1} = 2$$

$$LE_{N-NOR} = \frac{2N+1}{3}$$