

# Power

Monday, February 22, 2010  
09:17

## Total Energy

H → L → H (1 transition cycle)

$$E_{dynamic} = C_L V_{DD}^2$$

$$P_{dynamic} = C_L V_{DD}^2 f_{1 \rightarrow 0}$$

frequency of energy consuming transitions

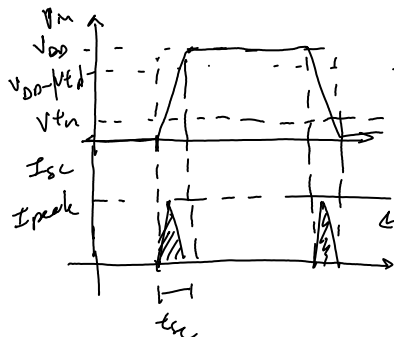
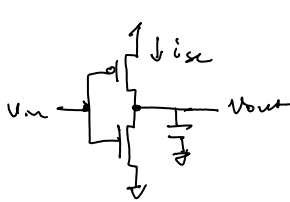
$$P_{dynamic} = C_L V_{DD}^2 f \cdot P_{1 \rightarrow 0 \text{ input}}$$

$$= V_{DD}^2 f \cdot C_{eff} \quad (C_{eff} = C_L \cdot P_{0 \rightarrow 1 \text{ output}})$$

To reduce  $P_{dynamic}$ :

freq ↓,  $V_{DD}$  ↓,  $C_L$  ↓

## Short Circuit Current



area of current through  
 $E_{sc} = \frac{1}{2} V_{DD} I_{peak} t_{sc}$

There are 2 triangles, so  
for the whole transition cycle

$$E_{sc} = V_{DD} I_{peak} t_{sc}$$

$$P_{sc} = V_{DD} I_{peak} t_{sc} f$$

Assuming linear rise/fall curve:

$$t_{sc} = \frac{V_{DD} - V_{Th} - |V_{Tp}|}{V_{DD}} \cdot t_{0 \rightarrow V_{DD}}$$

$$\approx \frac{t_r}{0.8}$$

rise time of input

Thus:

$$P_{sc} = V_{DD} I_{peak} f \frac{V_{DD} - 2V_T}{V_{DD}} \cdot \frac{t_r}{0.8}$$

How to reduce  $P_{sc}$ ?

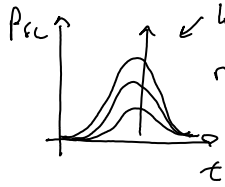
$$\Rightarrow V_{DD} \downarrow \quad V_{DD} < 2V_T$$

$$\frac{V_T}{L} \downarrow$$

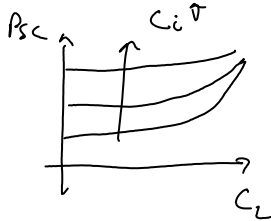
$$t_{r-bl}$$

make input switch  
super fast

If  $C_L$  is low enough, most of the energy goes to charge it up as opposed to short-circuiting.



raised  $P_{sc}$  (but decreases performance and causes power loss to charging it up)  
all we're doing is shifting the problem around



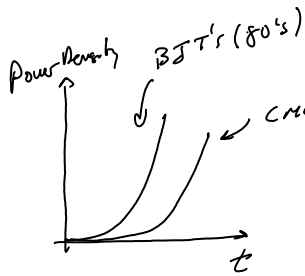
as your rise time increases ( $C_i$ ),  $P_{sc}$  gets worse

3 types of power

$P_{dynamic}$  → circuit is doing work, power loss is ok

$P_{sc}$  → sad, but mostly unavoidable

$P_{leakage}$  → almost equal to  $P_{dynamic}$  in deep submicron



We're in big trouble!

→ We're squeezing the last drops out of CMOS

by making CMOS power consuming stink