



# Static Power Reduction Techniques for Asynchronous Circuits

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# Power Constrained Design

- Static Power Reduction
  - Voltage Scaling
  - Threshold Adjustment
  - Power Gating

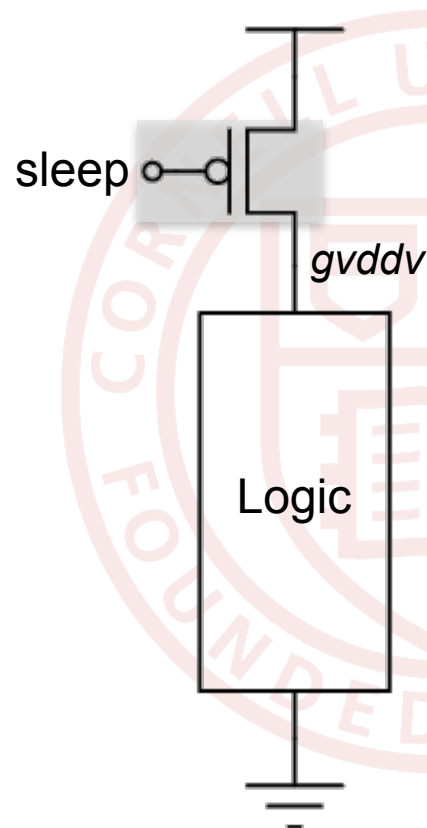
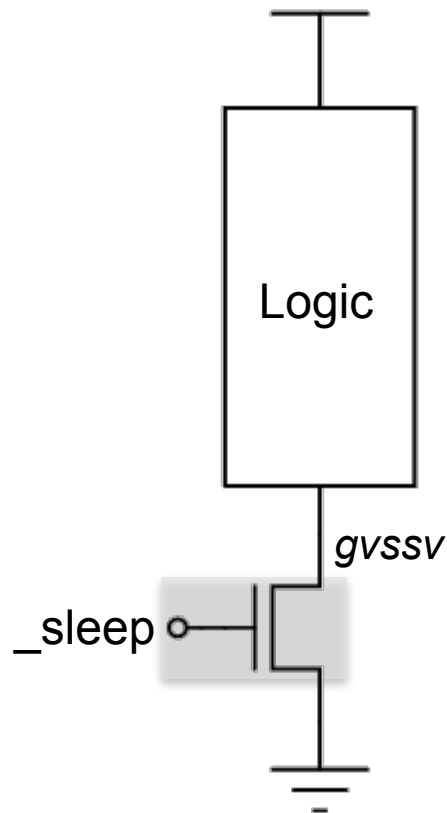


# Overview

- Power Gating Circuit Techniques
  - Non-state Preserving
  - State Preserving
- Asynchronous Power Gating Circuit Techniques
  - Non-state Preserving
  - State Preserving
- Pipeline Power Gating
  - Empty Pipeline Detection
  - Zero Delay Ripple Turn On (ZDRTO)
- Evaluations
- Conclusions



# Power Gating



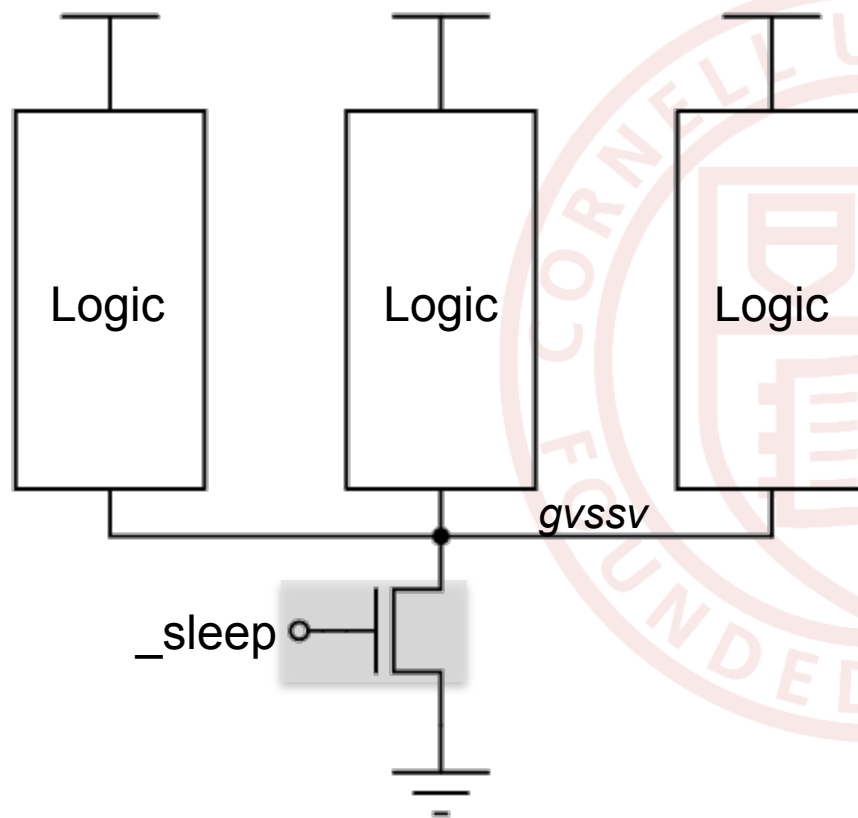
- Series Resistance
  - Leakage Reduction
  - Performance Penalty

- Virtual Power Nets
  - $gvddv$
  - $gvssv$

- Share Sleep Transistors



## Non-State Preserving Power Gating



- Cut-Off (CO)

- Internal Nodes Float

- nMOS Foot

- pMOS Head

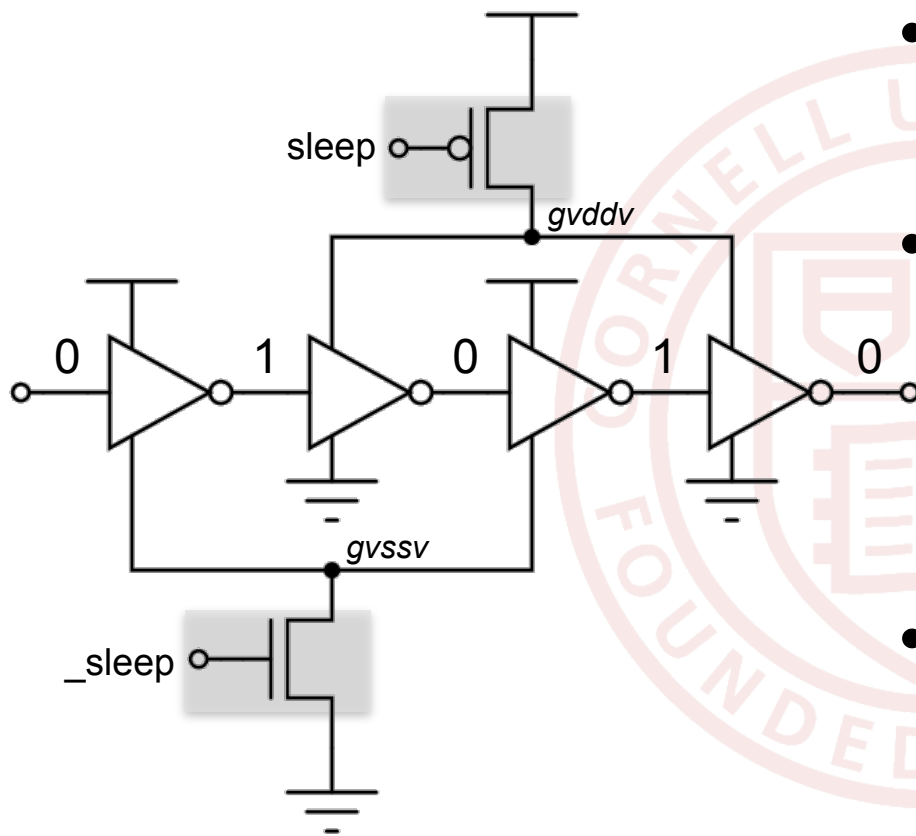
- Transient Behavior

- Long Sleep Settle Time

- Long Wakeup Time



## State Preserving Power Gating



- Zig-Zag Cut-Off (ZZCO)

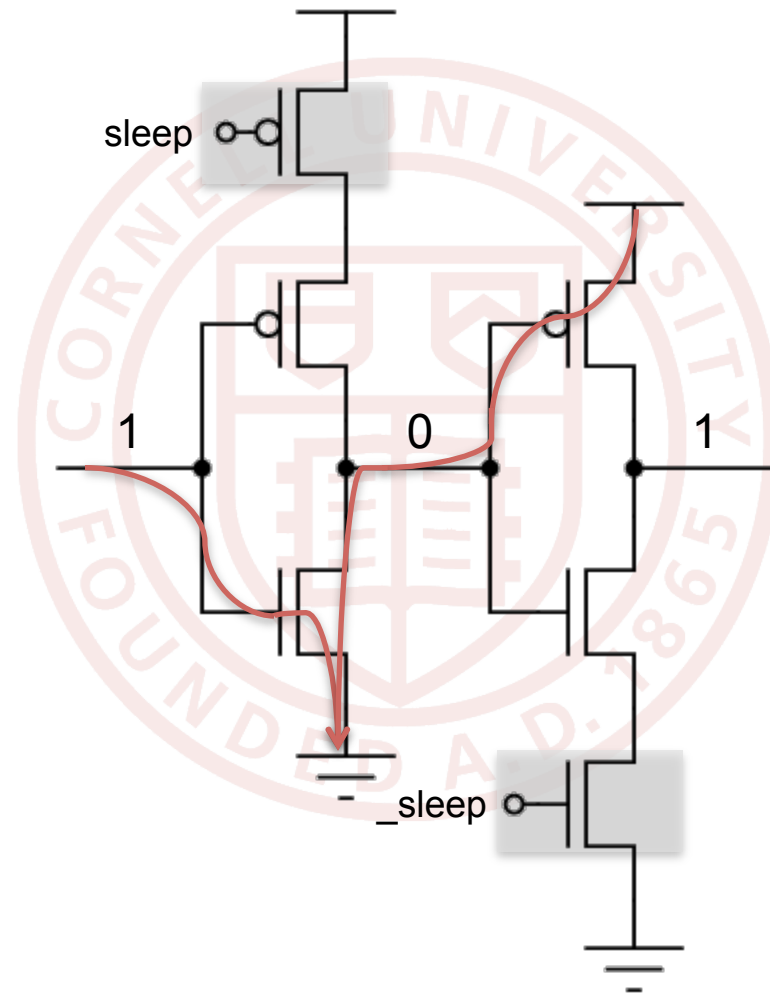
- Select Head or Foot
  - Head Transistor => 0
  - Foot Transistor => 1

- Better Transient Behavior vs. Cut-Off

- Worse Leakage



# State Preserving Power Gating





## Our Contributions

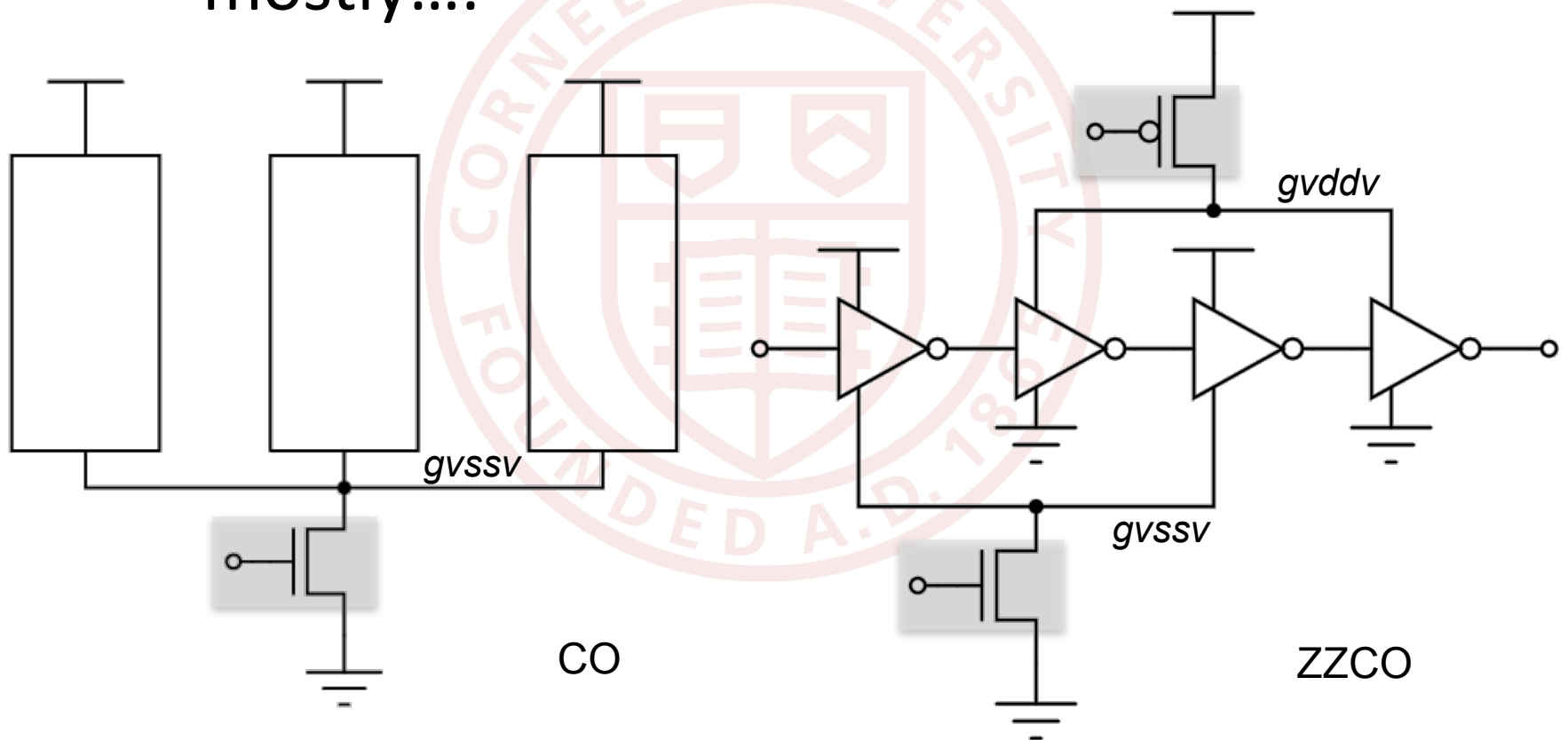
- Async Power Gating Circuit Techniques
- Pipeline Power Gating
  - Empty Pipeline Detection
  - Zero-Delay Ripple Turn On (ZDRTO)
    - Pipeline Power Up
    - Latency Hiding



# Asynchronous Power Gating

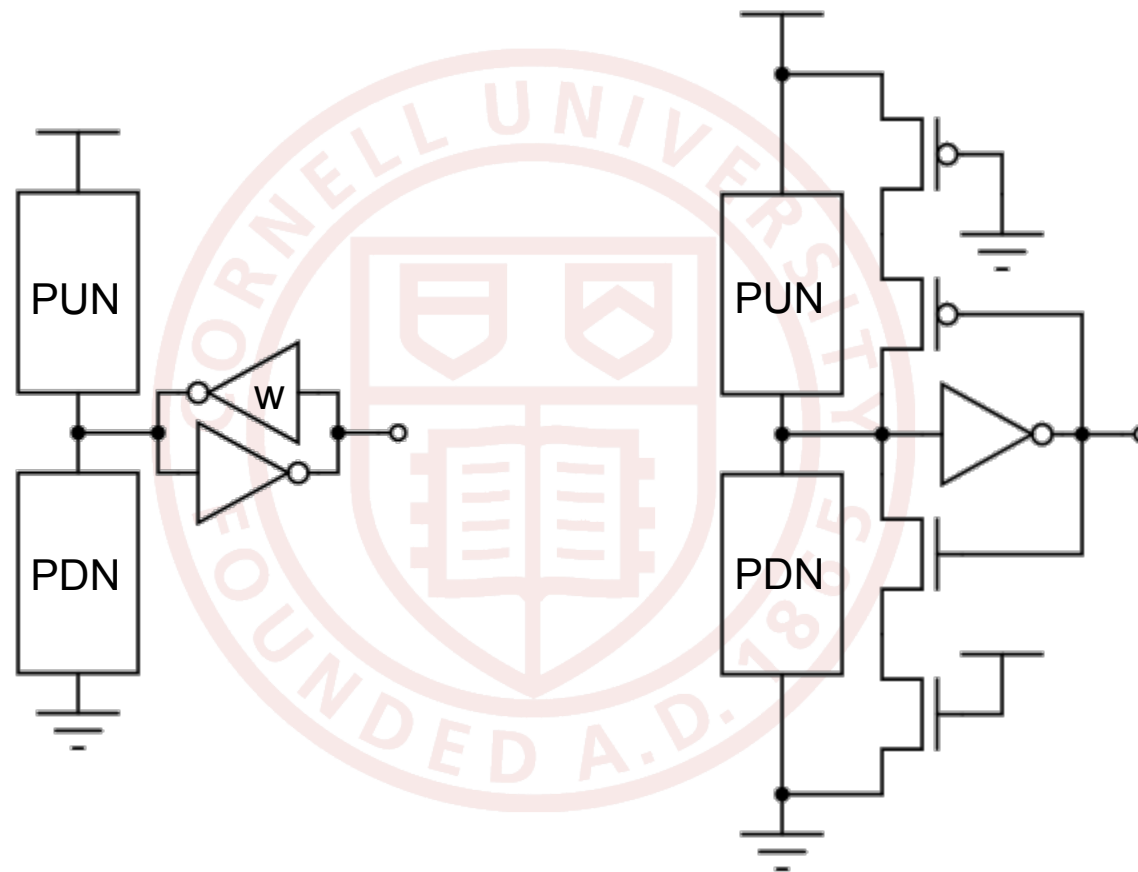
- Standard Techniques Work!

mostly....





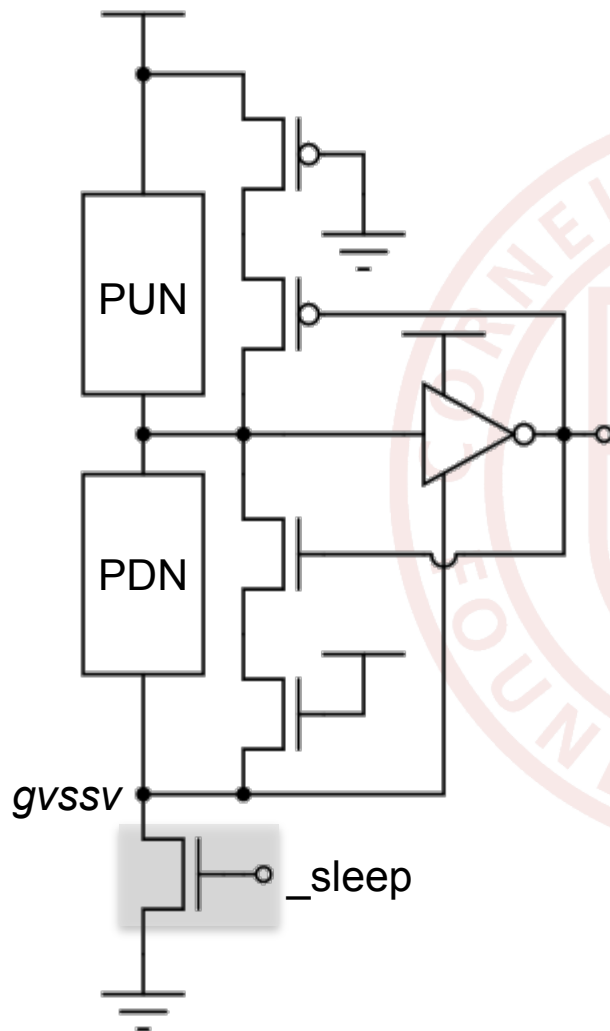
# Pseudo-Static Gates



Dynamic Gates with Staticizers



# Async Non-State Preserving Power Gating



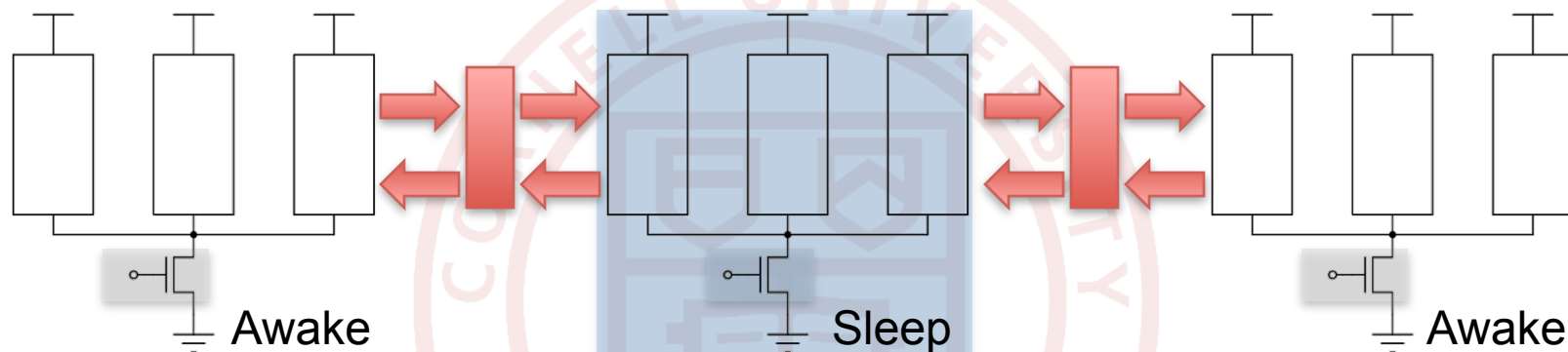
- Cut-Off (CO)

- Same approach
  - Static CMOS Gates
  - Pseudo-Static Gates



# Async Non-State Preserving Power Gating

- Isolation Circuits

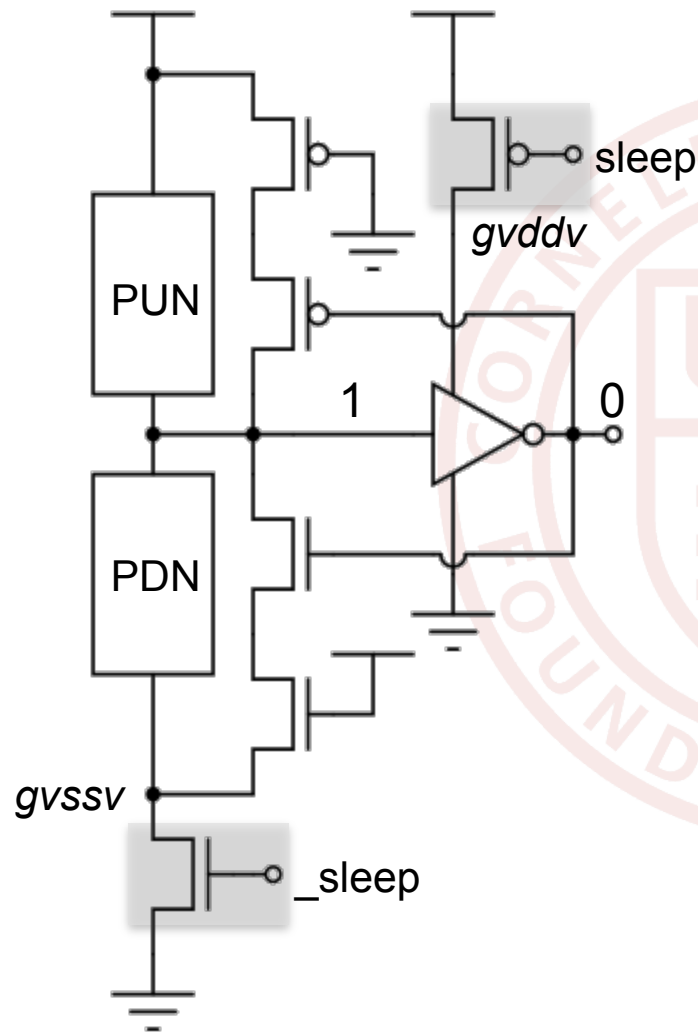


- Self Reset

- De-assert *sleep*
- Pulse *reset*
- Assert *safe*



# Async State Preserving Power Gating



- Zig-Zag Cut-Off(ZZCO)

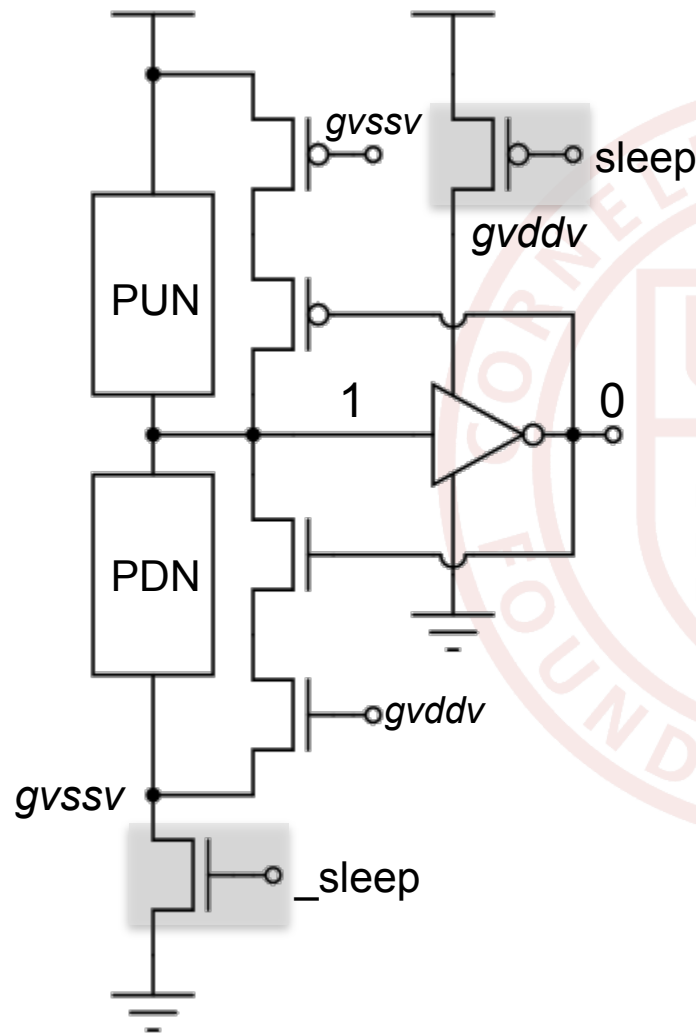
- Same approach

- Static CMOS Gates
- Pseudo-Static Gates

- Note Forward Inverter



## Async State Preserving Power Gating

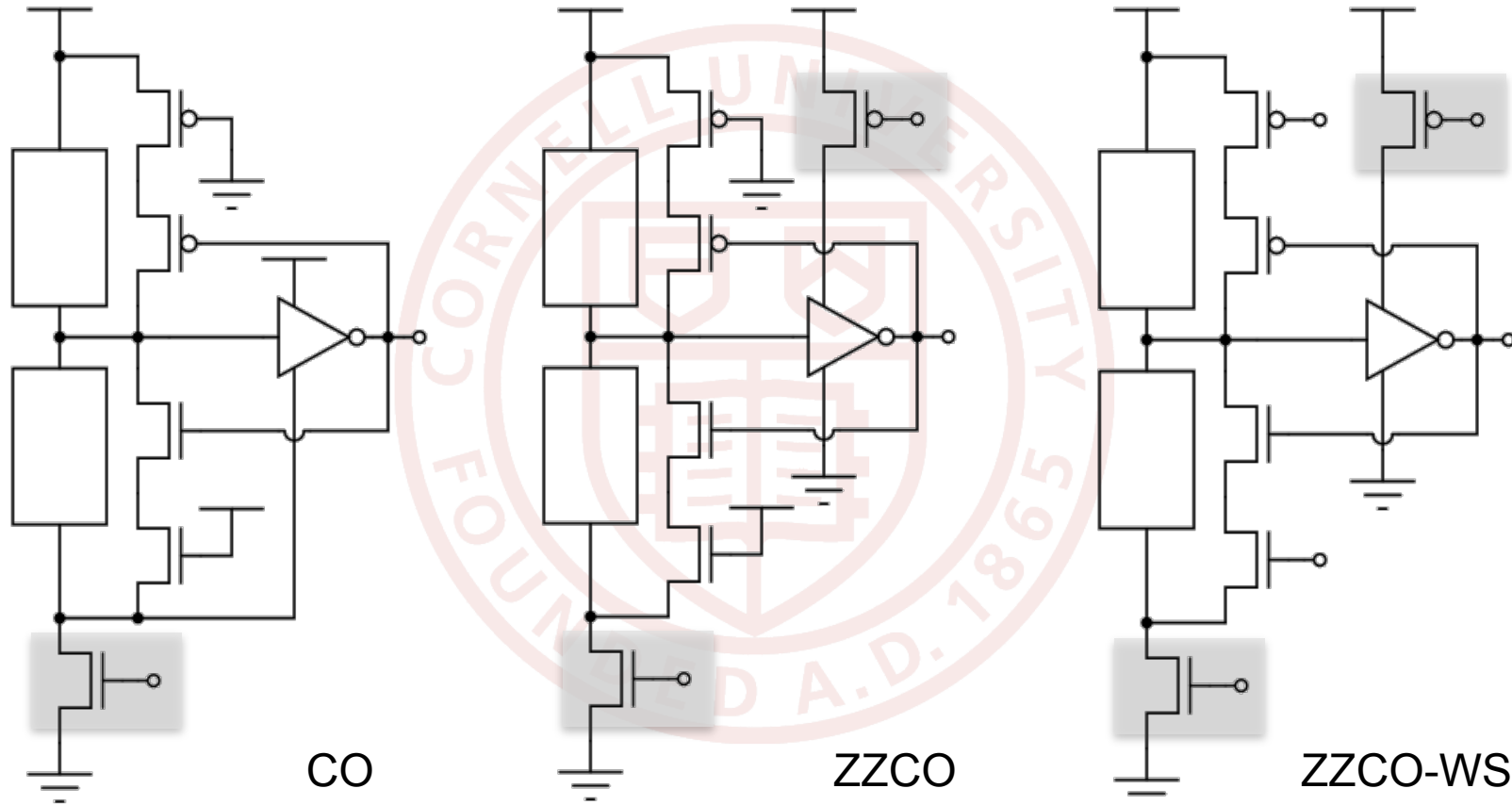


- Weakened Staticizer
  - gvddv instead of VDD
  - gvssv instead of GND
  - Better Power Savings
  - Better Performance

- Low-Cost
  - No Transistor Change
  - Different Netlist
  - Similar Wiring Costs



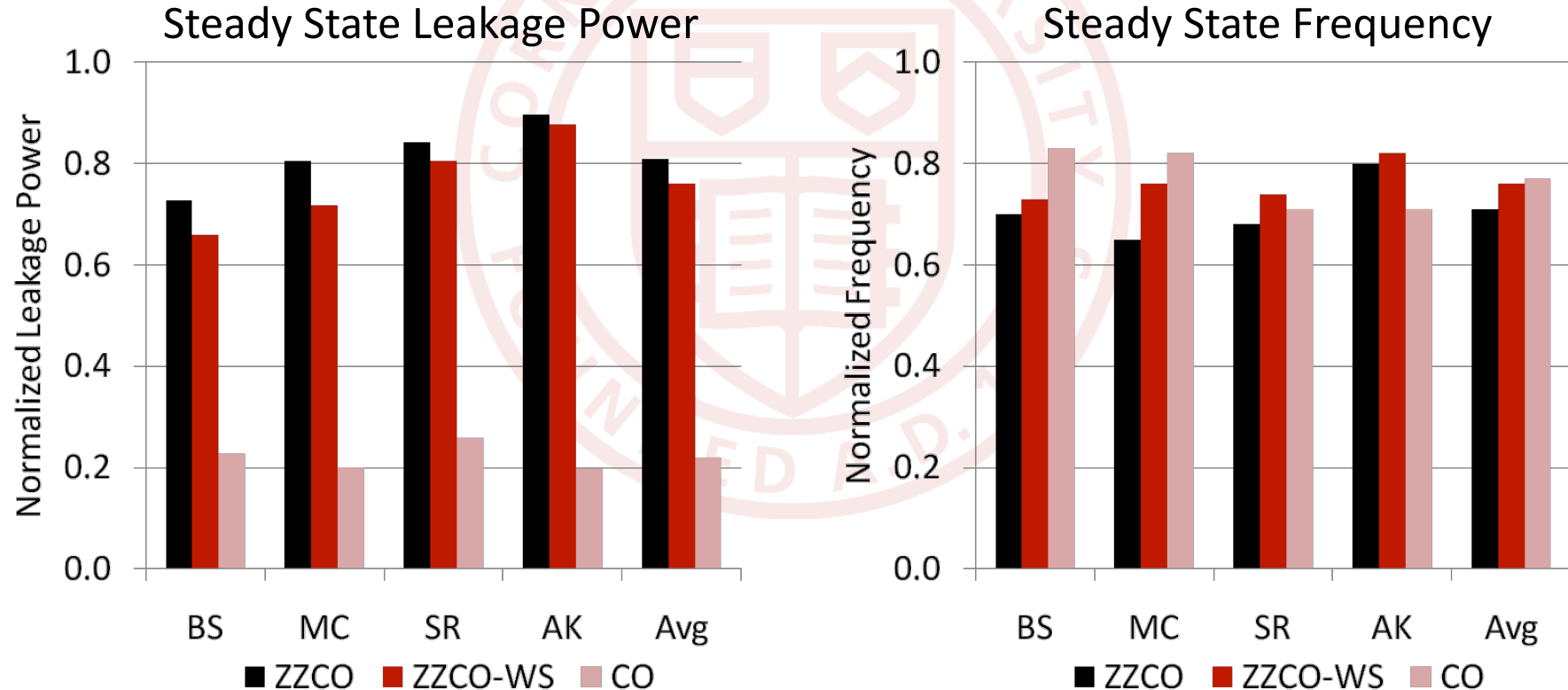
# Power Gating Circuit Techniques Evaluation





# Power Gating Circuit Techniques Evaluation

- BSIM4, T-T, Conservative Wire Cap, 90nm, 298K
- AES Pipeline Functional Blocks





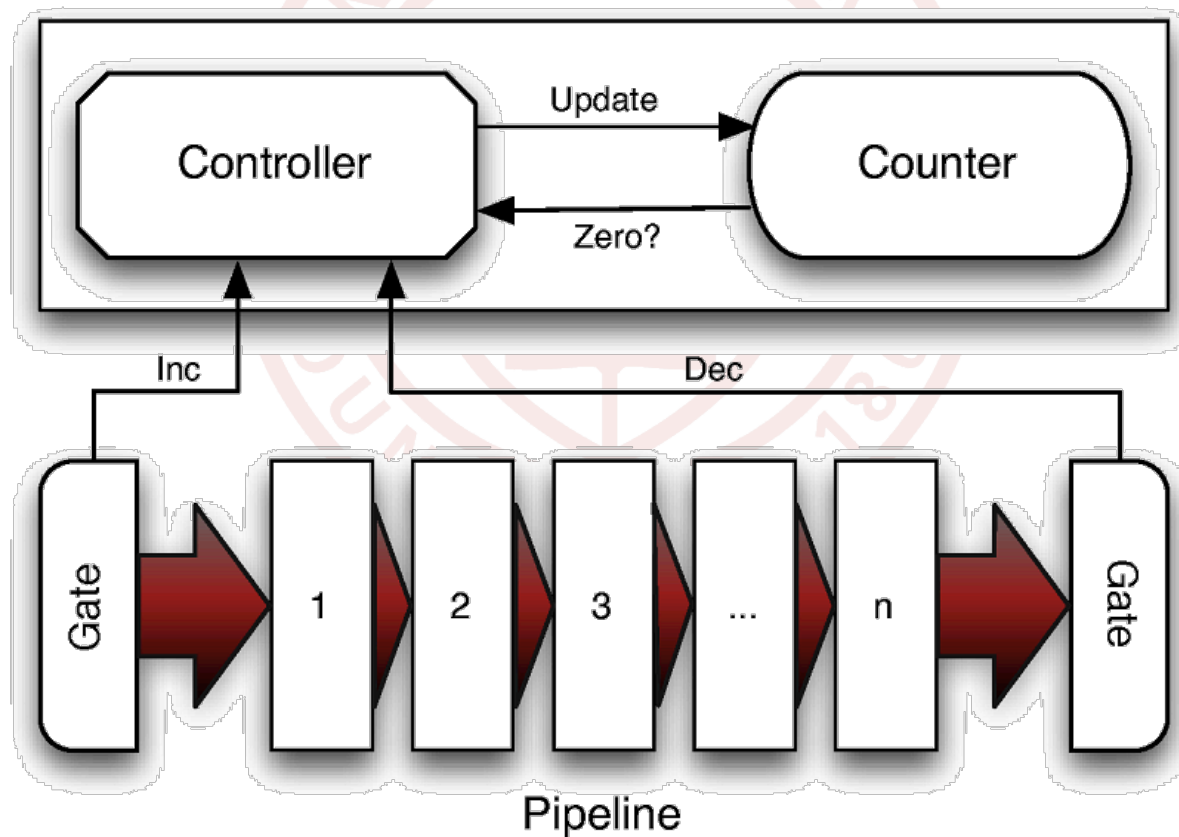
## Power Gating Techniques Evaluation

- CO offers the best **steady state**
  - Power Savings
  - Performance
- ZZCO-WS is better in steady state than ZZCO
  - Power Savings
  - Performance
  - Negligible Implementation Costs



## Empty Pipeline Detection

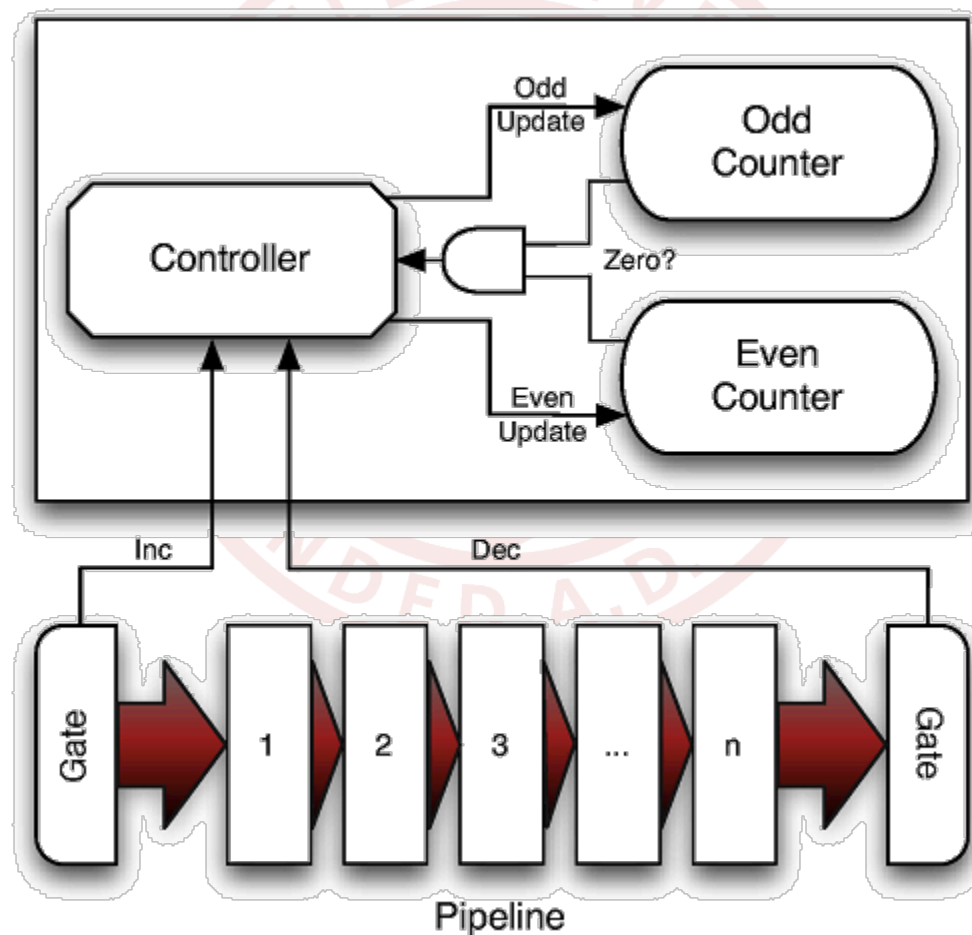
- Detect when it's safe to power gate
- Constant Response Time Counter





## Empty Pipeline Detection

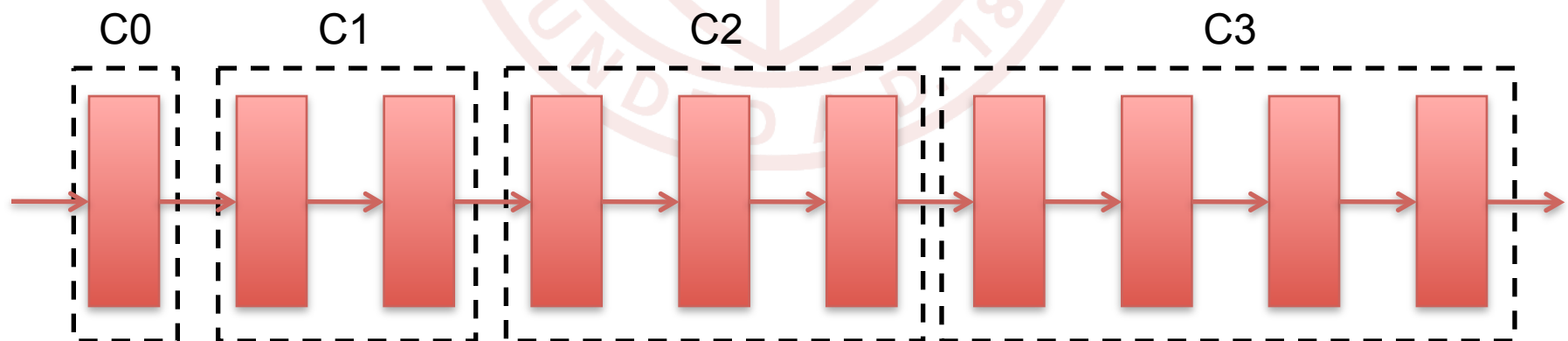
- To ensure full throughput, interleave counters





## Zero-Delay Ripple Turn On (ZDRTO)

- Pipeline Cluster = Power Gating Domain
- Choose
  - Pipeline Cluster sizings for your application
  - Power Gating techniques for each cluster

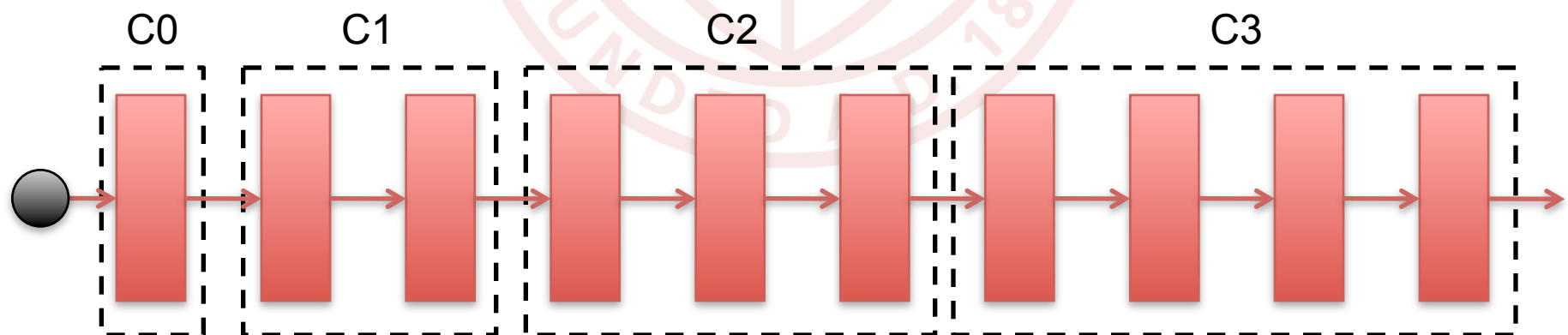


Pipeline Clusters



## Zero-Delay Ripple Turn On (ZDRTO)

- Leverage Pipeline Stage Computation Latency
  - Hide Latency of Powering Up Downstream Stages
- Leverage Asynchronous Circuit Robustness
  - Do Computation During Power Up



Pipeline Clusters



## ZDRTO Evaluation

- Results in Tradeoffs Between
  - Wake-Up Latency
  - Power Savings
  - Operating Frequency
- BSIM4, T-T, Conservative Wire Cap, 90nm, 298K
- Example Pipeline: 4-cluster AES Pipeline
- Different Power Gating Techniques



# ZDRTO Evaluation Pipeline Breakdown

Pipeline Clusters

| Pipeline Cluster      | Transistors   | FO4s      |
|-----------------------|---------------|-----------|
| Add Round Key (AK)    | 8400          | 2.4       |
| Shift Rows (SR)       | 7567          | 2.4       |
| Byte Substitute (BS)  | 84144         | 20.4      |
| Mix Column (MC)       | 30000         | 16.8      |
| AES Control Circuitry | 18000         | N/A       |
| Counter Overhead      | 4300          | N/A       |
| <b>Total</b>          | <b>152111</b> | <b>11</b> |

Power Gating Techniques

| No ZDRTO | AK   | SR   | BS   | MC   |
|----------|------|------|------|------|
| Baseline | None | None | None | None |
| CO       | CO   | CO   | CO   | CO   |
| ZZCO     | ZZCO | ZZCO | ZZCO | ZZCO |
| ZDRTO    | AK   | SR   | BS   | MC   |
| ZZ-ZDRTO | ZZCO | ZZCO | ZZCO | ZZCO |
| Mixed-A  | None | ZZCO | ZZCO | CO   |
| Mixed-B  | None | ZZCO | CO   | CO   |

Note that ZZCO is ZZCO-WS



## ZDRTO Evaluation Pipeline Breakdown

| No ZDRTO | Wake up (ns) | Leakage (uW) | Frequency (MHz) |
|----------|--------------|--------------|-----------------|
| Baseline | 0.0          | 7.10         | 285             |
| CO       | 32.9         | 1.50         | 262             |
| ZZCO     | 5.9          | 6.34         | 180             |

| ZDRTO    | Wake up (ns) | Leakage (uW) | Frequency (MHz) |
|----------|--------------|--------------|-----------------|
| ZZ-ZDRTO | 5.6          | 6.46         | 182             |
| Mixed-A  | 18.4         | 6.05         | 226             |
| Mixed-B  | 26.2         | 1.62         | 260             |



## Conclusions

- Asynchronous Power Gating Circuit Techniques
  - Non-state Preserving
  - State Preserving
  - 25-80% Savings
- Pipeline Power Gating Techniques
  - Empty Pipeline Detection
  - Zero-Delay Ripple Turn On (ZDRTO)
- Demonstrated Tradeoffs
  - Wake Up Latency
  - Power Savings
  - Operating Frequency



# Static Power Reduction Techniques for Asynchronous Circuits

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Acknowledgements:

- NSF, Blue Highway, Intel
- Derek Lockhart of Cornell CSL





## Power Gating Bias Techniques

- Bias Generators are Expensive
  - Can use current comparators
  - Complexity/area costs
- H.-J. Song. “A self-off-time detector for reducing standby current of DRAM.” IEEE SSC
  - Bias Generator
  - 115uW
- More Suitable for High-Power Circuit (HPC)

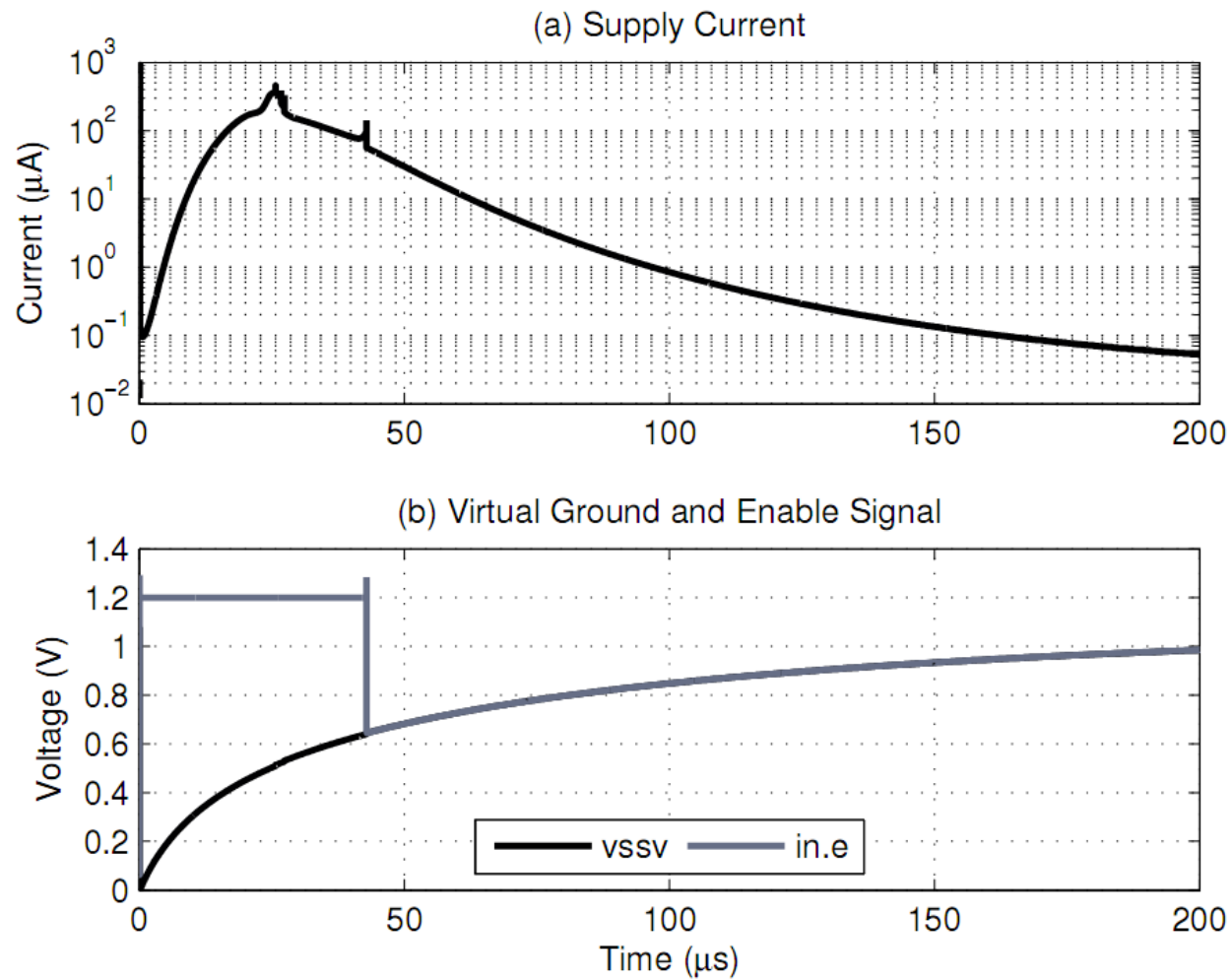


## Transistor Sizing

- Logic Optimized for
  - Energy
  - Static Power Reduction
- Kao, et al. “Transistor Sizing Issues and Tool for Multi-Threshold CMOS Technology.” IEEE DAC 1997



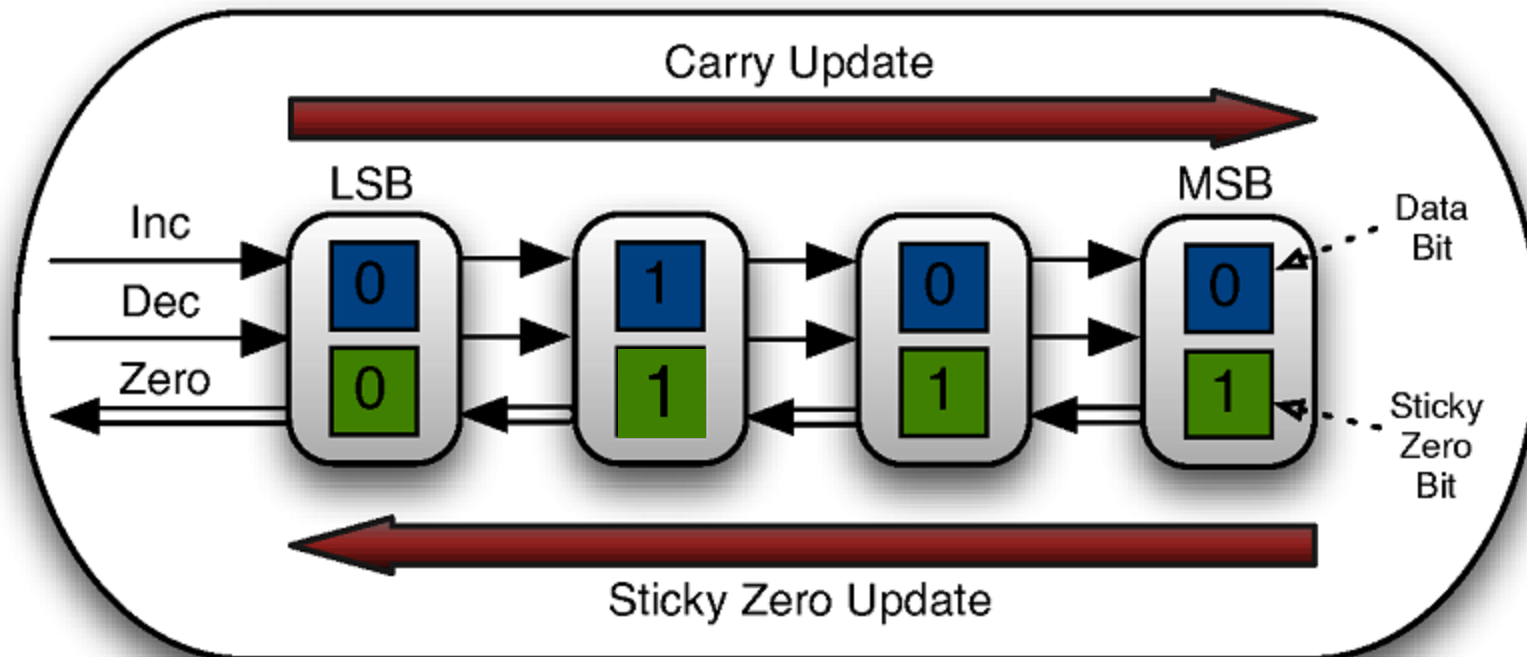
# Cut-Off Transient Behavior





# Constant Time Counter

## Counter



- Constant Time Response
- Simultaneous Increment/Decrement (Arbitration)



## Empty Pipeline Detection Overhead

- Shared Overhead (NRE)
- Per-Bit Overhead

|                  | Transistor Count | Static Power (nW) |
|------------------|------------------|-------------------|
| Shared Overhead  | 1900             | 95                |
| Per-Bit Overhead | 400              | 19                |



# Dynamic Power and Energy Overheads

|               | Dynamic Power (mW) | Energy Overhead |
|---------------|--------------------|-----------------|
| Baseline      | 18.97              | N/A             |
| CO            | 17.30              | -0.05%          |
| ZZ-ZDRTO      | 12.34              | 1.90%           |
| Mixed-A ZDRTO | 15.20              | 1.05%           |

Note:

Includes Empty Pipeline Detection and Isolation Circuit (when applicable) overheads.